ECE342 – Simulation Project

Jonathan Lam

December 9, 2020

Consider the following circuit:

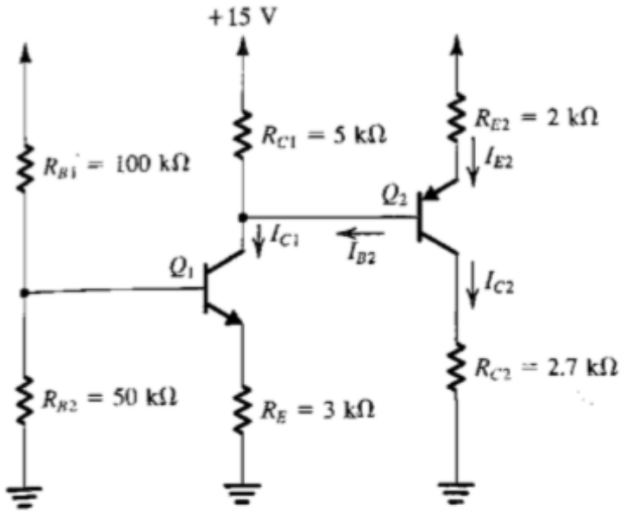

Figure 1: The circuit of consideration.

The transistor values are not given, so two common transistors were chosen: 2N2222 (NPN, Q_1) and 2N2907 (PNP, Q_2), which have corresponding LTSpice models. The values for these models are:

$$I_{S_1} = I_{S_2} = 10^{-14}\text{A}$$
$$\beta_1 = 200$$
$$\beta_2 = 250$$

1 Manual calculations

1.1 Solving for quiescent points

1.1.1 Solving for quiescent point of Q_1

Solve for V_{BE_1}, I_{C_1} numerically by iteration. Assume no early effect ($R_0 = \infty$), and assume that the base currents are negligible relative to the bias currents ($I_{B_1} \approx I_{B_2} \approx 0$). Alternate between the relations:

$$V_{BE_1} = V_T \log \frac{I_{C_1}}{I_{S_1}}$$
$$I_{C_1} = \frac{\beta_1}{\beta_1 + 1} \frac{V_{B_1} - V_{BE}}{R_{E_1}}$$

Using Python to perform the calculations, with initial values $V_{BE_{1_0}} = 0.7\text{V}$ and $I_{C_{1_0}} = 1\text{mA}$, we get the quiescent point for Q_1 (after 2 iterations):

$$I_{C_1} = 1.44\text{mA}$$
$$V_{BE_1} = 0.668\text{V}$$

With this, we can calculate the base current I_{B_1} to affirm our assumption that it is negligible relative to the bias current I_{bias_1} (the current through the biasing resistors):

$$I_{B_1} = \frac{I_{C_1}}{\beta_1} = \frac{1.44\text{mA}}{200} = 7.18 \times 10^{-6}\text{A} \ll 1.00 \times 10^{-4}\text{A} = \frac{15\text{V}}{100\text{k}\Omega + 50\text{k}\Omega} = I_{bias_1}$$

1.1.2 Solving for quiescent point of Q_2

We can use I_{C_1} to estimate the bias voltage V_{B_2} of the base of Q_2:

$$V_{B_2} = V_{C_1} = V_{CC} - I_{C_1} R_{C_1} = 15\text{V} - (1.44\text{mA})(5\text{k}\Omega) = 7.82\text{V}$$

Now we can calculate the quiescent point for Q_2:

$$V_{EB_2} = V_T \log \frac{I_{C_2}}{I_{S_2}}$$
$$I_{C_2} = \frac{\beta_2}{\beta_2 + 1} \frac{V_{CC} - (V_{B_2} + V_{EB_2})}{R_{E_2}}$$

Python is used to calculate the results again, using the same initial values ($V_{EB_{2_0}} = 0.7\text{V}$, $I_{C_{2_0}} = 1\text{mA}$). This gives:

$$I_{C_2} = 3.23\text{mA}$$
$$V_{EB_2} = 0.689\text{V}$$

Again, we can check that the base current I_{B_2} is indeed small relative to the bias current I_{C_1} (the current going through the first transistor):

$$I_{B_2} = \frac{I_{C_2}}{\beta_2} = \frac{3.23\text{mA}}{250} = 1.29 \times 10^{-5}\text{A} \ll 1.44 \times 10^{-3}\text{A} = I_{C_1}$$

1.2 Small signal model

The small signal model is simply two common-emitter topologies in series.

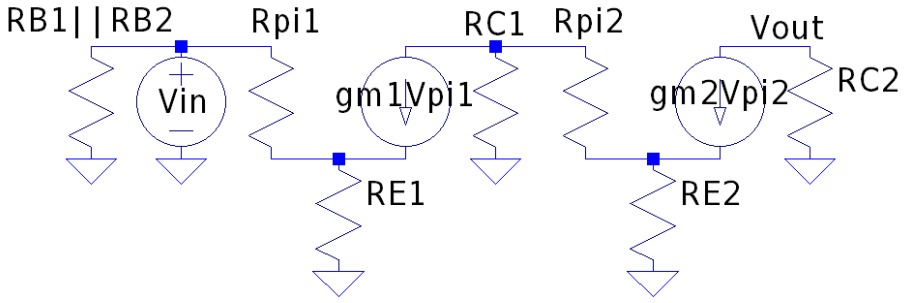

Figure 2: Small signal model

$$
\begin{aligned}
g_{m_1} &= \frac{I_{C_1}}{V_T} = \frac{1.44\text{mA}}{26\text{mV}} = 5.53 \times 10^{-2}\Omega^{-1} \\
R_{\pi_1} &= \frac{\beta_1}{g_{m_1}} = \frac{200}{5.53 \times 10^{-2}\Omega^{-1}} = 3.62 \times 10^{3}\Omega \\
g_{m_2} &= \frac{I_{C_2}}{V_T} = \frac{3.23\text{mA}}{26\text{mV}} = 1.24 \times 10^{-1}\Omega^{-1} \\
R_{\pi_2} &= \frac{\beta_2}{g_{m_2}} = \frac{250}{1.24 \times 10^{-1}\Omega^{-1}} = 2.01 \times 10^{3}\Omega
\end{aligned}
$$

1.3 Voltage gain

Rederiving the voltage gain of a common-emitter with emitter degeneration (and assuming no early effect):

$$
\begin{gathered}
\frac{V_\pi}{R_\pi} + g_m V_\pi = \frac{V_{in} - V_\pi}{R_E} \\
V_{out} = -g_m V_\pi R_C \\
V_\pi \left(\frac{1}{R_\pi} + g_m + \frac{1}{R_E} \right) = V_{in} \left(\frac{1}{R_E} \right) \\
\frac{V_{out}}{V_{in}} = -\frac{g_m R_C}{R_E \left(\frac{1}{R_E} + \frac{1}{R_\pi} + g_m \right)} = -\frac{-g_m R_C}{1 + \frac{R_E}{R_\pi}(\beta + 1)} = -\frac{R_C}{\frac{1}{g_m} + R_E \frac{(\beta+1)}{\beta}} \\
A_V \approx -\frac{R_C}{\frac{1}{g_m} + R_E}
\end{gathered}
$$

Intuitively, the input impedance for the common-emitter with emitter degeneration is $R_{in} = R_\pi + (\beta + 1)R_E$. In this example:

$$\begin{aligned}
A_V &= A_{V_1} A_{V_2} \\
&= \left[-\frac{R_{C_1} || R_{in_2}}{\frac{1}{g_{m_1}} + R_{E_1}} \right] \left[-\frac{R_{C_2}}{\frac{1}{g_{m_2}} + R_{E_2}} \right] \\
&= \frac{R_{C_1} || (R_{\pi_2} + (\beta_2 + 1)R_{E_2})}{\frac{1}{g_{m_1}} + R_{E_1}} \frac{R_{C_2}}{\frac{1}{g_{m_2}} + R_{E_2}} \\
&= \frac{5\text{k}\Omega || (2.01 \times 10^3 \Omega + (250 + 1)2\text{k}\Omega)}{\frac{1}{5.53 \times 10^{-2} \Omega^{-1}} + 3\text{k}\Omega} \frac{2.7\text{k}\Omega}{\frac{1}{1.24 \times 10^{-1} \Omega^{-1}} + 2\text{k}\Omega} \\
&= 2.21
\end{aligned}$$

2 LTSpice Simulation

2.1 Verifying the analytical results

See Figure 4 for the schematic used to check the quiescent points of Q_1 and Q_2, and 3 for the measured values.

See Figure 6 for the schematic used to check the small-signal voltage gain of the circuit, and 5 for the result. To measure the zero-centered voltage gain, a coupling capacitor and a large pull-down resistor $R_L = 1\text{M}\Omega$ were used (i.e., not a heavy load). The maximum amplitude of V_{in} and V_{out} were compared to calculate A_V.

I did not explicitly try to estimate the R_π and g_m values experimentally in LTSpice; the proximity of the calculated A_V to the true value is a good indicator that the calculated values are correct.

Overall, the experimental values were fairly close to the calculated ones. This reassures us that the assumptions made in the calculations were relatively safe to make ($I_{B_1} \approx I_{B_2} \approx 0$, $R_0 = \infty$).

	Calculated	Experimental
V_{BE_1}	0.668V	0.663V
I_{C_1}	1.44mA	1.35mA
V_{EB_2}	0.689V	0.685V
I_{C_2}	3.23mA	3.03mA
A_V	2.21	2.17

Table 1: Calculated vs. experimental metrics

2.2 Adding a load

When the load impedance R_L is made very small, we see that the voltage gain is catastrophically attenuated. It is not hard to see that the relationship between

R_L (Ω)	A_V (w/o EF)	A_V (w/ EF)
1	0.000804	0.122
2	0.00161	0.231
3	0.00241	0.329
4	0.00321	0.418
5	0.00401	0.497
6	0.00483	0.570
7	0.00563	0.637
8	0.00642	0.698
9	0.00722	0.755
10	0.00803	0.807

Table 2: Voltage gain after adding load with and without emitter-follower stage

A_V and R_L is roughly linear, which is expected from the voltage gain equation. ($A_V \propto R'_{C_2}$, where $R'_{C_2} = R_{C_2}||R_L \approx R_L$ (when $R_L \ll R_{C_2}$) when a load is attached.) A rough calculation shows that these values are expected: when $R'_{C_2} \approx 10\Omega$, $A'_V = 8.03 \times 10^{-3} \approx 8.19 \times 10^{-3} = \frac{10\Omega}{2.7\text{k}\Omega}(2.21) = \frac{R'_{C_2}}{R_{C_2}} A_V$.

The results are shown in Table 2.

2.3 Mitigating the effect of the load

To mitigate the effect of the load, we can use an additional emitter-follower stage before the load. While emitter-followers don't have a high gain, they have a much lower output impedance, so the gain will be attenuated less. Emitter-followers have the following output impedance:

$$R_{out} = \left(\frac{R_S}{\beta + 1} + \frac{1}{g_m}\right) || \, R_E$$

(derivation deferred to the textbook, where R_S is the resistance in series with the the base). The first term greatly decreases the output impedance. A common-emitter with emitter degeneration has output impedance $R_{out} = R_C$, which is much higher.

See the schematic in Figure 7. The results are shown in Table 2. It is clear that the gain is still significantly degraded, but is over a factor of 100 greater than the gain without the EF stage.

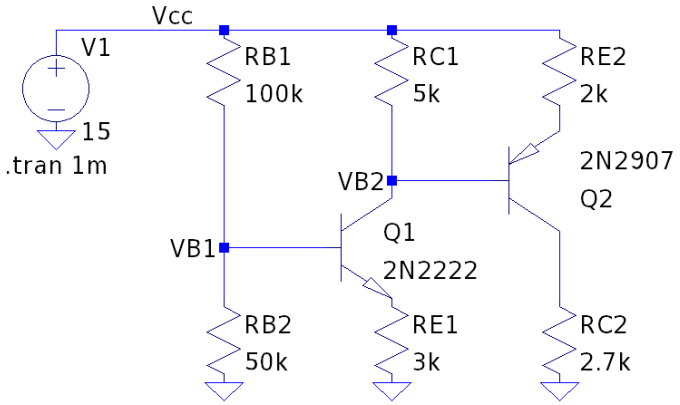

Figure 3: Biasing circuit in LTSpice, for checking the quiescent points of the transistors.

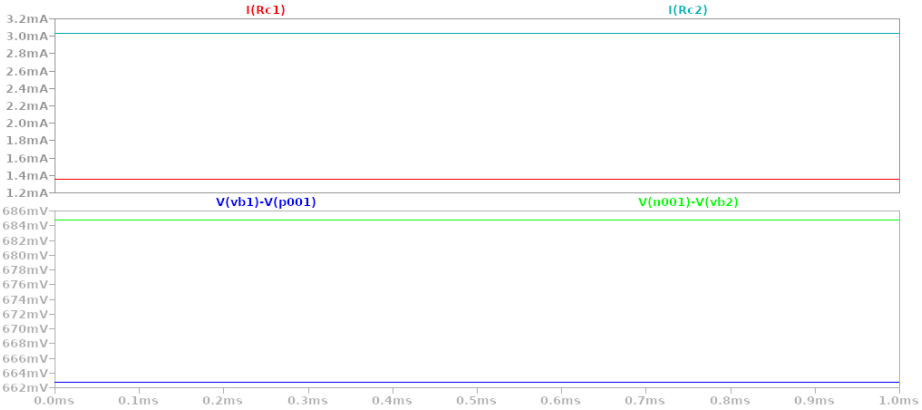

Figure 4: Quiescent points measured in LTSpice. Measured values: $I_{C_1} = 1.35\text{mA}$, $V_{BE_1} = 0.663\text{V}$, $I_{C_2} = 3.03\text{mA}$, $V_{EB_2} = 0.685\text{V}$.

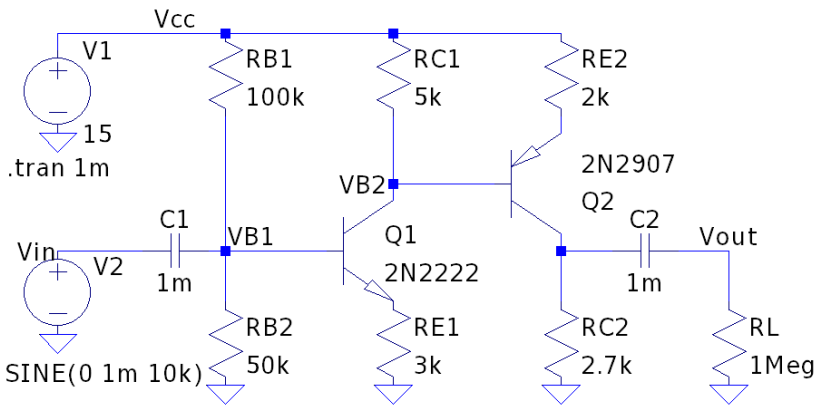

Figure 5: Circuit schematic in LTSpice. An input and output circuit with coupling capacitors are added to input and output a small, zero-DC-biased signal. Large coupling capacitors are used so that the small signals are not attenuated by much. The load resistor is large (1MΩ) when testing A_V so as to not load the circuit heavily.

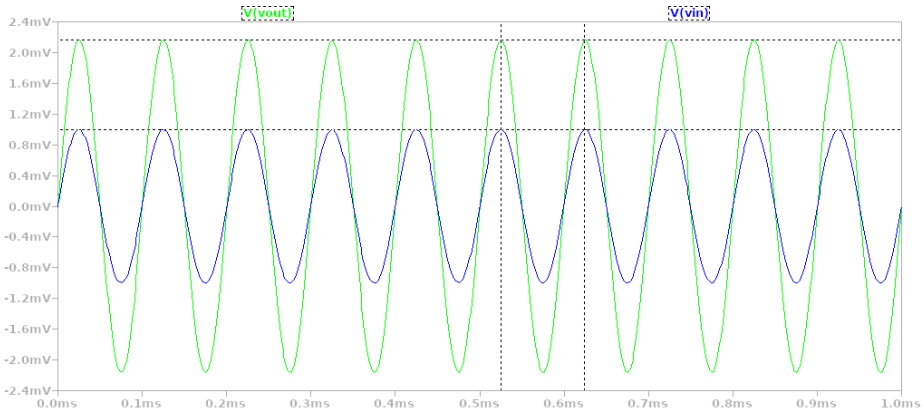

Figure 6: Two cursors placed at the maximum amplitudes of V_{in} and V_{out} when a small signal is applied. $V_{in} = 0.996\text{mV}$, $V_{out} = 2.16\text{mV}$; $A_V = 2.17$. (I also tried plotting V_{in}/V_{out}, but this causes numerical instability as $V_{out} \to 0$).

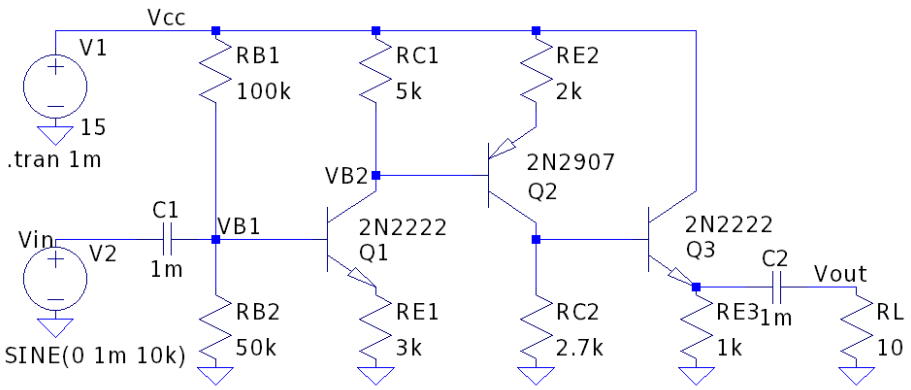

Figure 7: Schematic with emitter-follower stage to reduce output impedance, and thus be able to drive heavier loads (small R_L).